Superconductor digital electronics

Konstantin K. Likharev*

Department of Physics and Astronomy, Stony Brook University, Stony Brook, NY 11794-3800, United States

Contents lists available at SciVerse ScienceDirect

Physica C

A R T I C L E   I N F O

Article history:
Accepted 30 May 2012
Available online 15 June 2012

Keywords:
Cryotron
Josephson junction
Single-flux quanta devices
Reversible computing
Ultrafast computing
Supercomputing

A B S T R A C T

The objective of these notes is to offer a brief review of the history of superconductor digital electronics, and discuss prospects of its future development. Due to length restrictions, many important technical contributions could not be mentioned at all – with sincere apologies to their authors. Though an attempt has been made to give an unbiased review of the most important work all over the world, a special emphasis on the efforts in the former Soviet Union, which had not been discussed much in literature, and in which the author of this text took an active part, seemed excusable. Another important qualification is that the author phased out his own research in the field about 10 years ago, so that the last parts of the notes, devoted to present-time and future work, should be viewed as not much more than remarks by an (interested) outsider.

© 2012 Elsevier B.V. All rights reserved.

1. The cryotron age

The ideas of using superconductors for digital computing may be traced back at least to the famous paper [1] by D. Buck, then working in MIT Lincoln Laboratories. Fig. 1a shows the heart device of this idea, the cryotron. In this device, a coil made of a superconductor with a higher critical field was wound over a thinner “gate” wire made of a superconductor with a lower critical field. As a result, magnetic field induced by the supercurrent flowing in the coil might induce the superconducting-to-normal phase transition (i.e. control the resistance) of the gate wire which carried a larger current. From our present-day digital electronics experience, it is clear that such device is a virtually exact analog of a semiconductor field-effect transistor (besides that it operates with currents rather than voltages), and such active devices alone are sufficient to build any logic or memory circuit. For example, the circuit shown in Fig. 1b is an analog of a semiconductor SRAM cell.

Referring the reader to the classical book [2] by J. Brewer for a review of the initial work on cryotron circuits, let me mention just one their feature which is typical for virtually all superconductor digital devices: since a superconducting loop may carry persistent supercurrent for a practically unlimited time (while the circuit refrigeration keeps its temperature below \(T_c\)), cryotrons may be used to form nonvolatile memory cells. Moreover, it is easy to use them to form superconductor logic gates which store the operation result in the form of persistent supercurrent (and the associated magnetic flux). In comparison with mainstream semiconductor digital technologies (such as CMOS) where such storage requires special latch circuits, this feature creates additional conveniences for superconductor electronics.

The original D. Buck’s cryotrons were based on discrete, bulk components, hard to scale down below a few mm. As a result, their resistance \(R\) in the normal state was very low, and the typical inductance \(L\) rather high, so that the switching time scale \(\tau = L/R\) was of the order of \(10^{-4}\) s, and the original cryotron circuits could not compete in speed with other electronic devices available already at that time. However, just in a few month after D. Buck’s publication, an IBM team came up with the thin-film version of the cryotron (Fig. 2a) which enabled a dramatic improvement of cryotron circuit parameters. Indeed, since inductances of thin-film superconductor loops over a ground plane scales as \(\mu_0\sqrt{a}\) (where \(a\) is the insulator thickness and \(\mu_0\) is the London penetration depth [see, e.g., Section 3.09 in monograph [4]], and does not depend much on in-plane dimensions \(a\) (if they are much larger than \(t + 2\delta\), they immediately became almost as low as in modern superconductor circuits: \(L \sim 10^{-11}\) H. This is why even with a rudimentary lithography used for patterning of the first thin-film cryotron circuits (see, e.g., Fig. 2b), with \(a \sim 1\) mm, the switching time constant \(\tau\) shrank to \(10^{-8}\) s, though the critical current scale \(I_c \sim 1\) A and hence the energy dissipation scale \(E \sim I_c^2 t \sim 10^{-11}\) J/bit remained high.

Let me note, however, that if fabricated with the patterning readily available nowadays, say with the critical dimension \(a \sim 100\) nm, parameters of phase-transition-based cryotrons would rescale to \(I_c \sim 100\) mA, \(\tau \sim 1\) ps, and \(E \sim 10^{-19}\) J/bit, i.e. be very close to those of present-day Josephson-junction-based (say, RSFQ) circuits. This fact means that there is no impenetrable phy-
ics partition between these two approaches, and encourages a continuing search for intermediate superconductor device concepts, such as using non-tunnel Josephson junctions ("weak links" [5]), for example thin-film bridges or SNS sandwich structures.

2. The latching logic age

However, for the late 1960s and early 1970s, when nanoscale patterning was not available, the transfer to Josephson junction cryotrons, with their much lower values of \( I_c \) (and hence of \( E \) and \( \tau \) - as was confirmed in already the first sub-nanosecond switching time measurements [6]) has made a lot of sense. The first cryotrons of that type, demonstrated by J. Matisoo of IBM [7], had been exact replicas of the longitudinal thin-film cryotrons (Fig. 3), though later it was found that different “shaping” of long Josephson junctions [8], using lateral current injection into them [9], and replacing long junctions with two- or three-lumped junction interferometers [10] gives steeper critical current suppression curves. The dramatic reduction of \( I_c \) (to fractions of a milliamp) has also enabled to decrease the \( L/L_c \) products of superconductor loops (essentially, SQUIDs) to \( \sim \Phi_0 = h/2e = 2 \times 10^{-15} \text{ Wb} \), and hence use the magnetic flux quantization in superconducting loops to “clip” the stored variable to discrete values and as a result improve parameter margins of memory cells, with both destructive and non-destructive readout – see, e.g., Fig. 4.

Logic-circuit-wise, the most important new feature of the Josephson cryotrons was their high intrinsic capacitance, resulting in hysteretic \( I-V \) curves – see, e.g. Chapter 4 in monograph [11]. As a result, a current-biased junction “latches” in the resistive (R) state after its \( S \rightarrow R \) switching, and requires the bias current to be turned off to perform the junction reset, i.e. its reciprocal \( R \rightarrow S \) switching (Fig. 5). In order to cope with this feature, several families of “latching” Josephson logic circuits have been suggested – most of them by participants of a large-scale Josephson-junction computer project of IBM,¹ but with some important contributions by groups working in Bell Labs, Fujitsu Laboratories, NEC, and several university groups - notably including T. Van Duzer’s group in UC Berkeley. These latching logic families differed mostly by the way of the Josephson critical current suppression (including, in several versions, a direct injection of the control current into the junction or interferometer);² their common feature was the ac power supply which performed both the junction reset and logic gate clocking. The main challenge of this approach is that while the \( R \rightarrow S \) switching may be as short as a few picoseconds [13], the reciprocal \( S \rightarrow R \) switching is a complex dynamic phenomenon of Josephson phase trapping in a washboard potential (see, e.g., Section 5.3 in Ref. [11]) and requires, for realistic junction parameters, at least a few hundred picoseconds. As a result, the clock frequency of the latching logic circuits can be hardly increased far beyond 1 GHz. By the earlier 1980s it has become clear that such clock frequencies will be soon reached with semiconductor–transistor CMOS circuits which did not require helium refrigeration. As a result, the IBM project, which

¹ For a comprehensive review of this project, see the special issue of IBM J. Res. & Devel. of March 1980.

² A nice review of the latching logic work was given by S. Hasuo [12], so I refer the reader there for details.
dominated the field for almost 15 years, was shut down in the early 1983.

This development has not stopped the intensive research and development work in Japan, notably in Fujitsu Laboratories and NEC Tsukuba. An important aspect of the Fujitsu group work was the Josephson junction fabrication transfer from soft superconductors (such as lead alloys, used by IBM and NEC) to the “Nb-trilayer” (Nb/Al/AlOx/Nb) technology suggested earlier by J. Rowell, M. Gurvitch, and their colleagues in Bell Labs [14,15]. Such junctions feature a unique (and still not quite understood) self-organization of the 1-nm-scale AlOx layer (Fig. 6a) which enables their surprisingly repro-

---

**Fig. 3.** Longitudinal cryotrons based on (a) superconductor-to-normal phase transition and (b) Josephson junction’s critical current control [7].

---

**Fig. 4.** Generic single-flux-quantum memory cell with destructive readout, based on a dc SQUID: (a) schematics (with Josephson junctions indicated by red lines), and (b) basic operations shown on the $I_H$, $I_J$ plane. The solid point corresponds to the retention of binary data coded by the trapped magnetic flux quanta number $n$.

---

**Fig. 5.** Generic gate of the Josephson junction latching logic: (a) schematics and (b) two basic operations presented on the dc $[I, V]$ plane.

---

**Fig. 6.** Nb-trilayer Josephson junctions: (a) high-resolution TEM of the cross-section [12], and (b) dc $I-V$ curves of serial arrays of 500-nm junctions, demonstrating their low variability. (Picture courtesy by S. Tolpygo, HYPRES.).
ducible fabrication, with on-wafer variability of just a few percent (Fig. 6b). The Nb-trilayer junctions (after the perfection of their fabrication technology by Fujitsu – see, e.g., Ref. [12]) still remain the workhorse of all low-\(T_c\) superconductor electronics.

In the late 1980s this technology allowed the Fujitsu Laboratories team to demonstrate several relatively complex digital circuits such as an 8-bit digital signal processor with approximately 23,000 Josephson junctions, and energy consumption as low as \(\approx 1\) mW (Fig. 7). However, due to the same reset problems, the clock frequency of these circuits could not exceed 1 GHz, so that even such inspiring demos could not stop the demise of the latching logic which could not compete in speed with the emerging RSFQ circuits (see Section 4 below) or even with the rapidly improving CMOS technology. This was the main reason why the Fujitsu project was terminated in 1989. (Another one was the temporary fascination with the high-\(T_c\) superconductivity which seemed to mitigate the circuit refrigeration problem – see Section 5 below.)

3. Work in the Soviet Union

Let me interrupt the historic narrative to mention some Soviet work on superconductor electronics. From the 1930s, the USSR was stronger in low-temperature physics, in particular, in superconductivity, than in most other scientific fields, with major research centers in Moscow and Kharkov, and substantial groups in several other institutions. Naturally, its scientific establishment has reacted to the invention of cryotrons, with a strong group organized in Moscow-based Institute of Precision Mechanics and Computer Technology (Russian abbreviation ITMIVT), then famous for its BESM-4 and BESM-6 computers – probably the only Soviet success in computer technology, which was on a par with the Western competition of that time. The group has attracted some superb mathematics and circuit design talent such as S. Berkovich and G. Lapir (Fig. 8), and by 1964 came up with several original cryotron circuit ideas such as high-performance associative memories.

However, ITMIVT did not have an adequate technological base for the experimental implementation of these ideas, and in 1966 the core of the group (including both Berkovich and Lapir) joined the newly organized group in the Scientific Research Institute of Physi-

3 For more about this work, see S. Berkovich’s article [16].

Fig. 7. Fujitsu Labs’ 8-bit microprocessor with \(\approx 6300\) latching logic gates [12].

Fig. 8. The leaders of the Soviet work on cryotron circuits: (a) S. Berkovich (the first from the left) with his classmates at the entrance to Kapitsa’s Institute of Physics Problems in 1960, and (b) S. Berkovich (left) and G. Lapir visiting Novosibirsk’s Academic Town in 1966. Picture courtesy S. Berkovich (a) and G. M. Lapir (b).
non-latching, cryotron-type circuits. In particular, we came up with original schemes of current injection into the thin-film Josephson cryotrons (Fig. 10), which allowed to greatly increase the steepness of their “control characteristic” [9]. This work was patented in several countries (including the United States [18,19]), which was extremely hard to do due to rapidly worsening Soviet bureaucracy.4

Another focus of my work at that time was using flux quantization. From the late 1960s [20], it was clear that the effect could be used for memories, so I started to think about whether it may be used for logic operations as well. Due to my student research in parametric oscillations, I knew about E. Goto’s rf parametron invented as early as in 1954 [21]. A combination of these two ideas has led me, in early 1976, to the so-called parametric quantron [22]. This device (Fig. 11), later re-invented under the name of “quantum flux parametron” (QFP) [23], is essentially just an rf SQUID, biased by external flux $\Phi_0$ but with the Josephson junction’s critical current $I_0$ controlled by additional external current $I_c$. A combination of these two controls ($\Phi_0$ and $I_c$) allows not only the signal energy gain (which is necessary for logic devices) but even a physically reversible operation – thus providing a practical implementation of the general idea by Bennett [24]. In such reversible circuits, energy dissipation per bit may be well below the apparent “thermodynamic limit” $k_B T \ln 2$ and “quantum limit” $h/\tau$, where $\tau$ is the operation time [25].5

Encouraged by this invention, I have asked Rylov, at that time my MS student, to design a sizable reversible digital circuit based on parametric quantrons. This was a very hard task, but eventually it was accomplished – with a help provided by Semenov. (By that time, I have been able to find a research fellow line to have him hired back to MSU.) The result of their work [26] was rather disappointing: though such reversible circuits are possible, they require too much hardware to be practicable (e.g., almost $10^7$ parametric quantrons for an 8-bit, 1,024-point fast convolver) and, much more importantly, the speed of these circuits and their parameter variation tolerance is very low.6

4 In the 1970s, our NIIFP-MSU collaboration was probably the most active, but not the only Soviet group working on digital superconductor electronics. In particular, a sizable group was organized by I. Voitovich in the Institute of Cybernetics of the Ukrainian Academy of Science in Kiev. This group’s role in organizing annual summer schools on the subject in a wonderful recreation site Zhukin, in a pine forest on the bank of calm, warm, and clean Desna river, is especially memorable (Fig. 9b).

5 I have to note that my original paper [22] on that subject has had an essential error (namely, misidentifying the physical and informational reversibility) which was noted by Bennett and Landauer of IBM, who revealed it to me during my visit to Yorktown Heights in 1976. Fortunately, the error could be readily corrected [25].

6 Very unfortunately, these results were not taken into account by a Japanese collaboration working on flux quantum parametrons, who have arrived to similar conclusions almost 10 years later. Even more amazingly, the idea of computing using similar single-electron devices [27], re-invented later under the name of quantum-dot cellular automata (QCA) [28], are still pursued by several research groups!
4. The RSFQ age dawn

The disappointment with parametric quantron circuits by the mid-1980s has motivated us to think about other, simpler opportunities of computing with single flux quanta, forfeiting the reversibility option. By that time, several interesting efforts in this direction have been published. First, a Tohoku University group, led by K. Nakajima and Y. Onodera, suggested\cite{29,30} logic devices based on quantized vortex propagation in long transmission lines (Fig. 12). Literally taken, the suggestion was hardly practicable because of several reasons including the huge logic cell area (as expressed in minimum lithographic squares $F^2$), however, several circuit ideas (such as the single flux quantum splitting shown in Fig. 12a) were rather valuable because they could be readily reproduced with small, lumped junctions.

We were even more impressed by the experimental demonstration\cite{31}, by C. Hamilton and F. Lloyd of NIST Boulder, of the earlier idea by J. Hurell and A. Silver of TRW\cite{32} of dc SQUID switching by the so-called single-flux quantum (SFQ) pulses. It was clear from the early 1970s\cite{33} that such a pulse, with voltage "area"

$$\int V(t)dt = \Phi_0 = \frac{\hbar}{2e} \approx 2.07 \text{mV} \cdot \text{ps},$$

is the elementary result of integrating the Josephson voltage-to-phase relation

$$\frac{d\phi}{dt} = \frac{2e}{\hbar} V(t),$$

over a $\Delta \phi = 2\pi$ interval, so that it naturally (and unavoidably) appears across SQUID’s junction at its switching (say, by a slowly changing input current $I(t)$) into the adjacent flux quantum state (Fig. 13a). However, for a Josephson junction with a practicable critical current density (say, 1 kA/cm$^2$), externally shunted to avoid multi-quantum transitions, the SFQ pulse duration is about two picoseconds and its amplitude is about just $\sim 1$ mV (Fig. 13b). This is why the conjecture by Hurell and Silver that such a tiny pulse is sufficient to induce a similar flux transition in the following SQUID, even if transferred through a resistive wire (Fig. 13c), looked not too reliable. However, the NIST experiment\cite{31} has proved that such switching is indeed possible, at frequencies up to 100 GHz!

In the late 1984 I have got a new PhD student, O. Mukhanov, and asked him to pursue the SFQ pulse computing idea, working together with Semenov. Very soon, they suggested a full set of logic gates based on SFQ pulse switching\cite{34}. Following Hurell and Silver, SQUID loops in this first version were connected by resistors, so we decided to call the circuit family the Resistive Single-Flux-Quantum (RSFQ) logic. Very soon, it was found\cite{35} that the resistor replacement with an additional Josephson junction greatly improves parameter margins, but by that time we have so accustomed to the RSFQ acronym that decided to keep it, interpreting it as Rapid Single-Flux-Quantum logic.

The main idea of the RSFQ logic, schematically shown in Fig. 14, is that its flux-quantizing cells (by design, a few-junction SQUID loops, and in the computer design language, single-bit latches) communicate by SFQ pulses, i.e. “return-to-zero” voltage signals. Just as in the Hurell-Silver approach (Fig. 13), the SFQ pulses presenting input data and global clock are generated by (relatively) slowly changing external signals, but most pulses are developed at the RSFQ cell switching. At the circuit output, the SFQ-coded information is transferred to the usual (“non-return-to-zero”) voltage form by switching a quantizing dc SQUID. In contrast to latching logic, RSFQ circuits are powered by dc currents, thus avoiding the necessity in multi-GHz power lines.\footnote{Three of us had frequent and long discussions, so that possibly I provided some help (it is hard for me to remember details now), but the main credit for the idea belongs to Mukhanov and Semenov.}

Very excited by the RSFQ idea, I have approached V. Koshelets, my former student and at that time a head of a small experimental....
group at IRE (Institute of Radio Engineering and Electronics of the Soviet Academy of Sciences) with a kind request to try it – still in the resistively-coupled version. The result of our joint work was a very simple (2-superconductor-layer) integrated circuit shown in Fig. 15 [37], fabricated with 10 μm design rules. Despite such rudimentary technology, this self-testing circuit worked up to 30 GHz! At that time (1986), this was a world record of computing speed for any digital technology, and simple estimates [35] showed that scaling may allow to increase the clock frequency to a few hundred GHz. Not surprisingly, quite a few people in the Soviet Union (not known for many records in computing) were rather impressed. Very soon, these developments overlapped with another important news – the advent of high-\(T_c\) superconductivity.

5. High-\(T_c\) RSFQ?

The impact of the discovery of copper-oxide high-\(T_c\) superconductivity on the physics and electrical engineering community of the Soviet Union was similar (if not stronger) than that in the US and Japan. We even had a Moscow analog of the American “physics Woodstock”, held in Kapita’s Institute of Physics Problems in April.
1987. I was as excited as everybody, and even was the first in the country to observe Josephson effect in YBCO, using the second good sample synthesized by my friend A. Golovashkin of the Lebedev Institute, and kindly lent to me for one night. (Due to the rush, my liquid nitrogen cryostat was a matchbox!) The non-hysteretic $I-V$ curves of high-$T_c$ Josephson junctions, without any external shunting which was necessary for low-$T_c$ tunnel junctions, seemed a perfect match for RSFQ logic, while making the latching logic impossible – the fact our group liked a lot.

However, by the summer 1987 the excitement has calmed down, because the scale of enormous technological challenges faced by copper-oxide Josephson junctions became more clear. Using the fact that the main parameters of high-$T_c$ superconductors, including their London penetration depth $\lambda$, have been reliably measured by that time, I have recruited two of my MSU associates, Semenov and A. Zorin, to sit down, get sober, and estimate prospects of using such superconductors for high-temperature RSFQ logic and other applications in electronics, assuming that the fabrication challenges might be overcome.

The result was very simple, and very sad: no chance for RSFQ operating at “nitrogen” temperatures (~77 K) or higher. The main reason is that in order to avoid thermally-induced digital errors, critical currents of all junctions in RSFQ circuits have to be much (by a factor of 500 or so) larger than the current scale of thermal fluctuations (see, e.g., Chapter 1 of Ref. [11]):

$$ I_T = \frac{2e}{h} k_B T. $$

Fig. 17. The HTMT petaflops computer concept: (a) the general view (without the helium liquefaction unit, picture courtesy L. Bergmann, JPL) and (b) the RSFQ processing core design [47].
At the usual "helium" temperature of 4.2 K, this scale is close to 0.15 \( \mu \text{A} \), so that the smallest Josephson junctions may have critical current about 100 \( \mu \text{A} \). (Even in this case, the thermally-induced SFQ pulse jitter limits the maximum clock frequency of RSFQ circuits [38].) The 20-fold increase of temperature would require a proportional increase of \( I_c \). At the same time, the dimensionless SQUID inductance parameter
\[
\lambda \equiv \frac{2\pi}{\Phi_0} L_c,
\]
should be kept constant (for most circuits, \( \sim 3 \), but for certain loops, well below 1). As a result, any operation temperature increase has to be accompanied by a proportional decrease of loop inductances. But as was mentioned before, the lowest inductance available in thin-film superconductor circuits scales as
\[
L = l_0 (d + 2\lambda),
\]
where \( l \) is a dimensionless numerical factor which is already minimized in low-\( T_c \) RSFQ circuit layouts. Hence, even assuming that extremely small insulator thickness \( d \) is practicable, RSFQ circuit operating at 77 K would require a the London penetration depth \( \lambda \) of the order of 10 nm. In reality, \( \lambda \) of most copper-oxide superconductors is much larger than that level (even with supercurrent flowing in the most favorable \( ab \) plane) - and even larger than that of the most practicable low-\( T_c \) superconductor, niobium. Junction fabrication technology permitting, the known high-\( T_c \) superconductors may be used for operating complex RSFQ circuits at liquid-helium (or slightly higher) temperatures, but not 77 K.9

All this is very simple, but (at that time, very shockingly for na"ive me) the publication of our findings in the late 1987 (for its English version, see Ref. [40]) was met with open hostility by most of our Soviet Union colleagues and virtually ignored abroad, even after the arguments have been spelled out in our rather well-known review [41]. As a result, work on high-\( T_c \) digital circuits in some major laboratories continued until Year 2000 in the US, Year 2004 in Europe and Year 2007 in Japan (and still persists in some calmer harbors).

6. The RSFQ age

In late 1987, the NEC Tsukuba group in Japan published paper [42] reporting a new 1-kb Josephson memory decoder with decoding time of 280 ps – a solid but not an earthshaking result. However, an illiterate Pravda correspondent reported it in that leading Soviet newspaper as a superconductor memory performing 280 million of million operations per second (thus exaggerating the real speed by a factor of 280², i.e. by almost five orders of magnitude). His brief note has caught attention of the country’s leader M. Gorbachev, who has asked the USSR Academy of Sciences for a debriefing to the Soviet Politburo. Several well-positioned academicians were happy to speak to such an important audience about superconductivity research at large, but nobody of them knew much about superconductor electronics. As a result, E. Velikhov, Academy’s Vice-President, who had known about our group’s work through his part-time association with MSU, summoned lowly me for a 5 min talk at the debriefing in March 1988. I used that opportunity not only to explain the reporter’s error, but also to present our 30 GHz RSFQ result as a breakthrough, and an opportunity for the country to become a leader in ultrafast computing. The Politburo members were impressed, and as a result (with an essential help from Velikhov and his MSU associate A. Rakhimov who was my formal boss at that time), our MSU-IRE collaboration has got our research project funded on a level as high as \( \sim \$5 \text{M/year} \).

In spirit of the time, our project proposal promised some work on high-\( T_c \) Josephson junctions, a bit of superconductor-based single-electronics (which was another major success story of our group in the mid-1980s), but its real focus was the development of low-\( T_c \) RSFQ technology. We have succeeded to purchase about \$1 M worth of IC fabrication equipment for both MSU and IRE (some of which is still in use!) by the time the poor Soviet Union has got bankrupt in June 1990, and all our funding disappeared. With my background of being generally unhappy with the Soviet political system, I felt there was not much for me to do in the count-

---

9 Very simple circuits allow a little bit more permissive design and hence higher operation temperature [39].
try anymore, and used my long-planned visit to the US that summer to look for another accommodation for our RSFQ work.

By a lucky coincidence, exactly at that time, T. Berlincourt of the ONR has succeeded in pushing through the US DoD hierarchy a University Research Initiative (URI) topic on low-\(T_c\) digital electronics, whose BAA referred specifically to our Moscow RSFQ work – as something Americans should compete with! With that situation on hand, and substantial help from Stony Brook faculty (especially M. Gurvitch, J. Lukens and G. Sprouse), I have managed to arrange HYPRES’ hiring of the leading members of our RSFQ team (Mukhanov, Rylov, and Semenov), with myself landing at Stony Brook University where I could, within a few next years, transfer a group of talented Moscow students, notably including P. Bunyk, A. Kirichenko, S. Polonsky, P. Shevchenko, and D. Zinoviev.

With these human resources on hand, and HYPRES’ 1-kA/cm\(^2\) Nb-trilayer technology at our disposal, we easily won a sizable (~$1.2 M/year) 5-year project within Berlincourt’s URI topic, and started work on RSFQ implementation at earnest. By the end of the project, we have been able to pass all the way from single logic gates to rather complex circuits (such as the analog-to-digital converter with ~2,000 Josephson junctions shown in Fig. 16 [43]) which could operate at clock frequencies beyond 10 GHz.\(^{10}\)

We have also used the Stony Brook facilities of my friend Lukens to fabricate much simpler circuits with submicron, high-\(j_c\) junctions to demonstrate the real speed potential of RSFQ devices – such as a digital frequency divider operating up to 770 GHz, with power dissipation of only 1.5 \(\mu\)W [45]. To the best of my knowledge, this is still the world record for any digital technology; more importantly, such dynamic power consumption (~2 \times 10^{-18} \text{J/bit}) is some five orders of magnitude lower than that of high-speed semiconductor circuits. One may argue that this is power dissipated at 4.2 K, and a fair comparison with room-temperature electronics requires its multiplication by either the Carnot coefficient, about 10\(^2\), or the practical cryocoolers’ reciprocal efficiency, about 10\(^3\). However, even in the worst case, the RSFQ power advantage is still at least two orders of magnitude.

The early 1990s were the years of high excitement, the time when the RSFQ concept has gained a universal recognition in the superconductor electronics community, squeezing the latching logic and QFP circuits out of business.\(^{11}\) Unfortunately, by the end of the URI project in 1998, we started to feel the limitations of HYPRES’ fabrication technology: junction variability was too high, and only few copies (if any) of each new circuit worked, requiring enormous testing efforts. This is why I was desperately looking for funding sources which would allow us not only to continue the work on the same scale, but also get access to better fabrication technology. It looked like such opportunity was provided by the JPL-led Hybrid-Technology Multithreading (HTMT) computing project [46] whose declared finite goal was a petaflops computer with a compact RSFQ processing core (Fig. 17a). Though the scale of funding at the first stage of the project (1999–2000) was modest, with ~$1.2 M for our group, the

\(^{10}\) I can agree that the progress of S. Hasuo’s team at Fujitsu in the 1980s was even more spectacular, but RSFQ circuits require a more detailed design than the latching logic, and the development of adequate CAD software packages (such as PSCAN [44] and its cousins) took a lot of our time and effort.

\(^{11}\) Here I should note the very important role of our URI grant manager, H. Weinstock of the AFOSR, who was always very supportive of our work – even after the project has ended.
participants were assured that the “virtually guaranteed” funding scale for the next stage would be much larger and would allow us to use (or build our own) modern fabrication facilities.

With these prospects, our HTMT work was focused on the design of the switching network between ~4,000 RSFQ processors in the core, with a volume ~0.5 m³ (Fig. 17b). The network design (in contrast with that of processors as such) was very thorough, and we have managed to reduce the estimated average inter-processor latency to below 20 ns [47]. This number should be compared with the well-over-microsecond latency in existing petaflops-scale semiconductor computers, and shows why involving the Carnot-cycle efficiency in the dissipated power comparison may be misleading: the only power relevant to make the core so compact, and hence enable the small inter-processor latency, is that at 4.2 K, while all refrigeration (or rather helium liquefaction) is remote and does not interfere with core’s small size, low latency, and resulting high performance.

Unfortunately, by the end of Year 2000 it has become clear that we were misled by the project leaders: there was no funding in sight for its next stages, so that 2 years of our work were almost completely wasted. I was extremely frustrated. In addition, all my years at Stony Brook I was under a constant pressure of my other research ideas (including new nonvolatile memories, single-electron molecular devices, and hybrid CMOS/nano neuromorphic networks) for whose development the intensive RSFQ work left virtually no time. As a result, I have made a (possibly, wrong) decision to stop my work in superconductor electronics.

7. Recent trends

Since 2000, I had been following the further work in digital superconductor electronics very superficially, but after I had received a kind invitation to speak about it at the Superconductivity Centennial Conference in The Hague in September 2011, I had a good look at the current status of the field. What follows are my observation highlights:

(i) I see several RSFQ logic circuits (see, e.g., Fig. 18) with up to 10,000 Josephson junctions operating on frequencies up to 40 GHz [48,49], some simpler circuits operational up to 100 GHz [50], and SFQ RAMs designs up to 16 kb, with up to 80,000 junctions [51]. This progress has been possible due to the fabrication technology improvements including the transfer to higher critical current densities (up to 4.5 kA/cm² [52] or even 10 kA/cm² [53]), multilayer circuit planarization [50,51,53], and a substantial refinement of lithographic patterning which has resulted in much lower junction variability – see Fig. 6b. Still the integrated circuit progress during the past decade was not as impressive as I hoped for – apparently due to the very limited funding of the field.

(ii) Low-power helium-level cryocoolers with higher efficiency (approaching the Carnot cycle limit) have been used to demonstrate field systems with RSFQ chips [49,54] – see Fig. 19.

(iii) Several schemes for the reduction of RSFQ circuit power consumption have been suggested – for a critical review, see Ref. [55]. Of those, I like the ERSFQ scheme [56] in which the circuit components are powered by dc voltage (rather than dc current as in the original RSFQ version) developed across a special SFQ transmission line (Fig. 20a). Apparently, the hardware overhead is not forbiddingly large – see Fig. 20b.

(iv) There has been progress in development of digital superconductor circuits for picking up output signals from arrays of low-temperature sensors – see, e.g., Ref. [57]. The use of fast RSFQ circuits in such systems may help to time-division multiplex output signals from large-scale arrays, so that just one channel would be needed across the low-to-room temperature interface.

(v) There has been very interesting work on new Josephson junctions, in particular “p-junctions” with ferromagnetic interlayer [58] which may allow substantial savings of SFQ circuit area (which is especially important for memories) and increase their parameter margins, and SNS junctions with Nb, Si [59] and Ta, N [60] layers, which may eliminate the need in external shunts and as a result increase the RSFQ circuit density even further.

8. Future prospects

There is little doubt that the use of RSFQ circuits for some scientific and special applications will continue. However, prospects for capturing much larger markets, for example, large-scale ultrafast computing, are more questionable. Any attempt to capture that market would involve an uphill battle against the CMOS technology which is getting an enormous leverage from the consumer electronics market. (A bit exaggerating, the economy of modern electronics is ruled by texting teenagers rather than thinking scientists.)

Still, I believe that the RSFQ technology, with its large advantage in speed (more exactly, circuit latency), and an even larger advantage in low power consumption, has a chance to become a very serious player in supercomputing. For that to happen, the super-
References


